REMARKS

Claims 1-4 have been examined on their merits and are all the claims pending in the application.

1. Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Blinne et al. (U.S. Patent No. 5,274,568) in view of Hasegawa (U.S. Patent No. 6,041,168) (hereinafter Hasegawa '168) and in further view of Hasegawa (U.S. Patent No. 5,528,511) (hereinafter Hasegawa '511).

The initial burden of establishing that a claimed invention is *prima facie* obvious rests on the USPTO. *In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984). To make its *prima facie* case of obviousness, the USPTO must satisfy three requirements:

1. The prior art relied upon, coupled with the knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated to artisan to modify a reference or to combine references. *In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988).
2. The proposed modification of the prior art must have had a reasonable expectation of success, and that determined from the vantage point of the artisan at the time the invention was made. *Amgen, Inc. v. Chugai Pharm. Co.*, 927 F.2d 1200, 1209 (Fed. Cir. 1991).
3. The prior art reference or combination of references must teach or suggest all the limitations of the claims. *In re Vaeck*, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991); *In re*

Wilson, 424 F.2d 1382, 1385 (CCPA 1970).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, the nature of a problem to be solved. *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999). Alternatively, the motivation may be implicit from the prior art as a whole, rather than expressly stated. *Id.* Regardless if the USPTO relies on an express or an implicit showing of motivation, the USPTO is obligated to provide particular findings related to its conclusion, and those findings must be clear and particular. *Id.* A broad conclusionary statement, standing alone without support, is not "evidence." *Id.; see also, In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001).

In addition, a rejection cannot be predicated on the mere identification of individual components of claimed limitations. *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000). Rather, particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. *Id.*

Blinne et al. disclose, *inter alia*, a method of estimating propagation delay times associated with integrated circuit logic cells. Blinne et al. disclose an emulation technique that determines the propagation delay of a rising signal edge or a falling signal edge through a logic cell. *See* col. 1, lines 45-48 of Blinne et al. The Examiner acknowledges that Blinne et al. fail to teach or suggest logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of a plurality of circuits. *See*

June 16, 2003 Final Office Action, page 3. The Examiner alleges that Hasegawa '168 supplies the necessary disclosure to overcome the acknowledged deficiencies of Blinne et al.

Hasegawa '168 discloses, *inter alia*, a high-speed delay analysis apparatus that uses nodes and arcs to determine propagation delay within a circuit. Hasegawa '168 considers external pins and circuit element pins to be nodes, and signal flow between the nodes is considered to be an arc. *See* col. 3, lines 26-28; Fig. 3 of Hasegawa '168. Propagation delay times between two adjacent nodes are stored in the arc connecting the two adjacent nodes. *See* col. 3, lines 30-33; Fig. 4 of Hasegawa '168. To determine the propagation delay between a node at the input of the circuit and a node at the output of the circuit, the delay values stored in the consecutive arcs along the path between the input node and the output node are added together. *See, e.g.*, col. 5, lines 24-33; Figs. 5 and 6 of Hasegawa '168. The Examiner alleges that it would have been obvious to combine Blinne et al. with Hasegawa '168 in order calculate delay time based upon logic information, connection information and delay information. The Examiner acknowledges, however, that the combination of Blinne et al. and Hasegawa '168 fail to teach or suggest logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of a plurality of circuits. *See* June 16, 2003 Final Office Action, page 4. The Examiner alleges that Hasegawa '511 supplies the necessary disclosure to overcome the acknowledged deficiencies of the combination of Blinne et al. and Hasegawa '168.

Hasegawa '511 discloses, *inter alia*, a delay time verification method that provides propagation delay times even when the rising edge or the falling edge of a signal is meaningless. *See*

col. 2, lines 63-65 of Hasegawa '511. The method disclosed by Hasegawa '511 uses nodes and arcs in a fashion similar to Hasegawa '168. *See, e.g.*, col. 5, lines 16-23 of Hasegawa '511.

With respect to claim 1, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to teach or suggest a delay analysis library comprising delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information. The combination of Blinne et al., Hasegawa '168 and Hasegawa '511 does not use input signal transition and logical state information in the same manner as the present invention. In the present invention, delay times are based upon the current logical state of a logic circuit, and type of input signal transitions that are present on the inputs of the logic circuit. A rising edge signal might have two different propagation delay times, based on the logical state of the circuit and the logical states of the other input signals. On the other hand, Blinne et al. are concerned with the propagation time of a rising or falling edge through a logic cell. *See* col. 1, lines 45-48 of Blinne et al. Blinne et al. do not teach or suggest determining delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state. Blinne et al. ignore the logic operation of the analyzed logic circuit by independently recording each of the many inputs of the logic circuit. Inputs not being measured are fixed to a predetermined logic level while measuring the delay time of the remaining input. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne et al. In calculating the maximum delay time for the logic circuit, Blinne et al. uses the delay time of the input with the *longest* delay time. For example, this delay time is longer than what would be found in normal AND gate operation, because in that case the output falls as soon as the input with the shortest delay time falls. Hasegawa '168

does not even disclose signal transitions, but instead adds a series of maximum delay times together to determine a propagation delay. *See* col. 5, lines 23-34; Fig. 5 of Hasegawa '168. While the circuit modeling technique disclosed by Hasegawa '511 uses rising and falling signals, Hasegawa '511 still rely upon maximum delay times, stored in the arcs between nodes, for propagation delay time calculations. *See* col. 6, lines 54-56 of Hasegawa '511. Hasegawa '511 does not teach or suggest determining delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state. The combining of Blinne et al., Hasegawa '168 and Hasegawa '511 with each other does not remove this fundamental deficiency which permeates each of the references. In the three references, the propagation delay time for a logic circuit is arrived at using maximum delay times, and there is no discussion of using the input signal transitions and the current logical state of the logic circuit as index to a propagation delay time that is representative of how the logic circuit actually operates.

In addition, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to teach or suggest that a delay time is selected from delay time information according to input terminal signal transition type and current logical state of a circuit, as recited in claim 1. The Examiner acknowledges that Blinne et al. fail to teach or suggest this feature of the present invention.[1] The Examiner alleges that Hasegawa '511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne et al. As discussed above, Hasegawa '511 does not teach or

[1] It is clear that Hasegawa '168 fails to teach or suggest this feature of the invention as well, since the analysis method disclosed in Hasegawa '168 does not involve signal transitions or the logical operation of the modeled circuit.

suggest determining delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state. Instead, Hasegawa '511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations. Unlike the present invention, Hasegawa '511 does not differentiate between the type of signal transition at the input of a logic circuit when determining a delay time, and Hasegawa '511 does not use both the type of signal transition and the logical state of a logic circuit when selecting a delay time for a particular signal propagation through the logic circuit.

Thus, Applicants believe that the Examiner cannot fulfill the "all limitations" prong of a *prima facie* case of obviousness with respect to claim 1, as required by *In re Vaeck.*

Since Blinne et al., Hasegawa '168 and Hasegawa '511 do not disclose a delay analysis library comprising delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information, Applicants believe that one of skill in the art would not be motivated to combine the three references. *In re Dembiczak* and *In re Zurko* require the Examiner to provide particularized facts on the record as to why one of skill would be motivated to combine the two references. Without a motivation to combine, a rejection based on a *prima facie* case of obviousness is improper. *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998)). The level of skill in the art cannot be relied upon to provide the suggestion to combine references. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308 (Fed. Cir. 1999). The Examiner must make specific factual findings with respect to the motivation to combine references. *In re Lee*, 277 F.3d 1338, 1342-44 (Fed. Cir. 2002).

Although the Examiner provides a generalized motivation analysis with respect to a delay analysis method, none of the references disclose providing delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information. As discussed above, Blinne et al., Hasegawa '168 and Hasegawa '511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne et al.; col. 5, lines 23-34; Fig. 5 of Hasegawa '168; col. 6, lines 54-56 of Hasegawa '511. In addition, none of the references teach or suggest that a delay time is selected from delay time information according to input terminal signal transition type and current logical state of a circuit, as recited in claim 1. Since none of the references teach or suggest these features of claim 1, Applicants submit that one of ordinary skill in the art would not have been motivated to combine the three references. Thus, Applicants believe that the Examiner cannot fulfill the motivation prong of a *prima facie* case of obviousness with respect to claim 1, as required by *In re Dembiczak* and *In re Zurko*.

Based on the foregoing reasons, Applicants believe that the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to disclose all of the claimed elements as arranged in claim 1. Therefore, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 clearly cannot render the present invention obvious as recited in claim 1. Thus, Applicants believe that claim 1 is in condition for allowance. Applicants respectfully request that the Examiner withdraw the § 103(a) rejection of claim 1.

With respect to claim 2, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to teach or suggest a delay analysis library comprising delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information. As discussed above with respect to claim 1, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 does not use input signal transition and logical state information in the same manner as the present invention. In addition, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to teach or suggest selecting a delay time between an input terminal and an output terminal of a logic circuit from stored delay time information according to input terminal signal transition type and current logical state of logic circuit. The Examiner acknowledges that Blinne et al. fail to teach or suggest this feature of the present invention.[2] The Examiner alleges that Hasegawa '511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne et al. As discussed above with respect to claim 1, Hasegawa '511 does not teach or suggest determining delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state. Instead, Hasegawa '511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations. Unlike the present invention, Hasegawa '511 does not differentiate between the type of signal transition at the input of a logic circuit when determining a delay time, and

[2] It is clear that Hasegawa '168 fails to teach or suggest this feature of the invention as well, since the analysis method disclosed in Hasegawa '168 does not involve signal transitions or the logical operation of the modeled circuit.

Hasegawa '511 does not use both the type of signal transition and the logical state of a logic circuit when selecting a delay time for a particular signal propagation through the logic circuit.

Thus, Applicants believe that the Examiner cannot fulfill the "all limitations" prong of a *prima facie* case of obviousness with respect to claim 2, as required by *In re Vaeck.*

Since Blinne et al., Hasegawa '168 and Hasegawa '511 do not disclose a delay analysis library comprising delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information, Applicants believe that one of skill in the art would not be motivated to combine the three references. None of the references disclose providing delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information. As discussed above with respect to claim 1, Blinne et al., Hasegawa '168 and Hasegawa '511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne et al.; col. 5, lines 23-34; Fig. 5 of Hasegawa '168; col. 6, lines 54-56 of Hasegawa '511. In addition, none of the references teach or suggest selecting a delay time between an input terminal and an output terminal of a logic circuit from stored delay time information according to input terminal signal transition type and current logical state of logic circuit, as recited in claim 2. Since none of the references teach or suggest these features of claim 2, Applicants submit that one of ordinary skill in the art would not have been motivated to combine the three references. Thus, Applicants believe that the

Examiner cannot fulfill the motivation prong of a *prima facie* case of obviousness with respect to claim 2, as required by *In re Dembiczak* and *In re Zurko*.

Based on the foregoing reasons, Applicants believe that the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to disclose all of the claimed elements as arranged in claim 2. Therefore, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 clearly cannot render the present invention obvious as recited in claim 2. Thus, Applicants believe that claim 2 is in condition for allowance. Applicants respectfully request that the Examiner withdraw the § 103(a) rejection of claim 2.

With respect to claims 3 and 4, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to teach or suggest referencing a delay analysis library comprising delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information. As discussed above with respect to claim 1, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 does not reference a delay analysis library comprising input signal transition and logical state information that is formulated in the same manner as the present invention. In addition, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to teach or suggest selecting a delay time is selected from delay time information according to input terminal signal transition type and current logical state of a circuit, as recited in claims 3 and 4. The Examiner

acknowledges that Blinne et al. fail to teach or suggest this feature of the present invention.[3] *See* June 16, 2003 Final Office Action, pages 8 and 10, respectively. The Examiner alleges that Hasegawa '511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne et al. As discussed above with respect to claim 1, Hasegawa '511 does not teach or suggest determining delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state. Instead, Hasegawa '511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations. Unlike the present invention, Hasegawa '511 does not differentiate between the type of signal transition at the input of a logic circuit when determining a delay time, and Hasegawa '511 does not use both the type of signal transition and the logical state of a logic circuit when selecting a delay time for a particular signal propagation through the logic circuit.

Thus, Applicants believe that the Examiner cannot fulfill the "all limitations" prong of a *prima facie* case of obviousness with respect to claims 3 and 4, as required by *In re Vaeck.*

Since Blinne et al., Hasegawa '168 and Hasegawa '511 do not disclose a delay analysis library comprising delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information, Applicants believe that one of skill in the art would not be motivated

[3] It is clear that Hasegawa '168 fails to teach or suggest this feature of the invention as well, since the analysis method disclosed in Hasegawa '168 does not involve signal transitions or the logical operation of the modeled circuit.

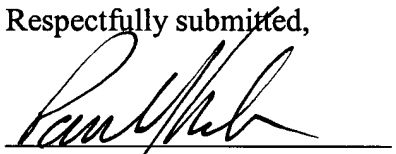
to combine the three references. None of the references disclose providing delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information. As discussed above with respect to claim 1, Blinne et al., Hasegawa '168 and Hasegawa '511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne et al.; col. 5, lines 23-34; Fig. 5 of Hasegawa '168; col. 6, lines 54-56 of Hasegawa '511. In addition, none of the references teach or suggest selecting a delay time is selected from delay time information according to input terminal signal transition type and current logical state of a circuit, as recited in claims 3 and 4. Since none of the references teach or suggest these features of claims 3 and 4, Applicants submit that one of ordinary skill in the art would not have been motivated to combine the three references. Thus, Applicants believe that the Examiner cannot fulfill the motivation prong of a *prima facie* case of obviousness with respect to claims 3 and 4, as required by *In re Dembiczak* and *In re Zurko*.

Based on the foregoing reasons, Applicants believe that the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to disclose all of the claimed elements as arranged in claims 3 and 4. Therefore, the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 clearly cannot render the present invention obvious as recited in claims 3 and 4. Thus, Applicants believe that claims 3 and 4 are in condition for allowance. Applicants respectfully request that the Examiner withdraw the § 103(a) rejection of claims 3 and 4.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: September 4, 2003